i)

Modules AND\_ONE and AND\_TWO use two different Verilog styles.

AND\_ONE uses the behavioral style, which utilizes assign statements to set variables.

ex: assign p = a & b;

AND\_TWO uses the structural style, which utilizes logical statements to set variables.

ex: and g0(p,a,b);

ii)

Synthesizing AND\_ONE will not result in the same structure as AND\_TWO. Being of the structural style, AND\_TWO describes the specific hardware implementation to be created during synthesis. Behavioral code simply defines the end result, but not how to get there, so the synthesizer may create a different hardware implementation.